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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,959	AVIZIENIS, ALGIRDAS	
	Examiner	Art Unit	
	Bryce P. Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL OFFICIAL ACTION

Status of the Claims

Claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64 and 65are rejected under 35 USC §112, second paragraph.

Claims 4, 16, 26, 36, 47, 59, 63 and 66 are rejected under 35 USC §112, fourth paragraph.

Claims 48 is rejected being a duplicate of claim 43.

Claims 1-15, 17, 18, 20-23, 25, 26, 28-31, 42-46, 48, 49, 52, 53, 55-58, 60 and 62 are rejected under 35 USC §102.

Information Disclosure Statement

All IDS is now properly considered.

Duplicate Claim Objection

Claim 48 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 43. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64 and 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64 and 65, the Examiner is unable to determine the bounds of "substantially exclusively made up of substantially commercial, off-the-shelf components." The Examiner is unable to determine a reasonable limit to the claims. For example, is a stock commercially available processor which has been over clocked 1% substantially off-the-shelf? What if the same processor has over clocked by 20%, is the resulting processor still off-the-shelf? What a user modifies a product against the manufacturer's wishes, as disabling the frequency clocking protections and over clocking a processor? At what point does the increased possibility of failure due to modification render a device no longer substantially exclusively commercially, off-the-shelf? Is the degree of commercial, of-the-shelf determined by the amount of effort, time or money used to modify element? At what point does the effort, time or money render an element no longer substantially commercial or off-the-shelf.

Rejections under 35 USC §112, fourth paragraph

The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

Claims 4, 16, 26, 36, 47, 59, 63 and 66 are rejected under 35 USC §112, fourth paragraph as they fail to further limit the scope of the claims. The *such computer system* of these claims is each case has already been claimed verbatim in the parent claim. These claims recite a "such computer." Each claim depends from a parent claim containing in the preamble: "failure of a computer system." Each parent claim then recites the failure in the body of the claim. As the failure is recited in the body of the claim, the descriptors from the preamble breath life into the bodily recited limitation and warrant patentable weight. As the Examiner is then required to find the computer system, reciting "such computer system" in its own claim becomes a redundant limitation; and when presented singularly fails to meet eh requirements of §112, fourth paragraph, namely that a dependant claim must further limit the parent.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-15, 17, 18, 20-23, 25, 26, 28-31, 42-46, 48, 49, 52, 53, 55-58, 60 and 62 are rejected under 35 U.S.C. 102(e) as being anticipated by Rasmussen (United States Patent No. 6,754,846 B2).

As per the claims, Rasmussen discloses:

1. Apparatus for deterring failure of a computing system; said apparatus comprising:

hardware network of components, having substantially no software (column 3, lines 9-18);

terminals of the network for connection to such system (connections to devices require a "terminal" as the connections connect at terminals to the devices);

fabrication-preprogrammed hardware circuits of the network for guarding from failure (column 4, lines 46-53).

2. Apparatus of the claim 1, particularly for use with such system that is substantially exclusively made up of substantially commercial, off-the-shelf components; and wherein:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient failure of such system (column 10, lines 43-51); and

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal (column 2, lines 33-38).

3. The apparatus of claim 2, wherein:

the circuits comprise portions fabrication pre-programmed to evaluate the at least one error signal to establish characteristics of the at least one recovery signal (column 2, lines 33-38).

4. The apparatus of claim 1, wherein:

such computing system (see claim 1).

5. The apparatus of claim 1, wherein:

the circuits comprise portions for identifying failure of any of the circuits and correcting for the identified failure (column 10, lines 42-61).

6. The apparatus of claim 1, particularly for use with a computing system that has at least one software subsystem for conferring resistance to failure of the system (column 2, lines 4-5); and wherein:

the circuits comprise substantially no portion that interferes with such failure resistant software subsystem (no interference is disclosed, clearly no interference is intended, and substantially does not require complete disclosed non-interference).

7. Apparatus of the claim 1, particularly for use with such system that is substantially exclusively made up of substantially commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein:

the circuits comprise portions for reacting to said response of such hardware subsystem (column 2, lines 33-38).

8. The apparatus of claim 1, particularly for use with a computing system that has plural generally parallel computing channels; and wherein:

the circuits comprise portions for comparing computational results from such parallel channels (column 2, lines 5-8).

9. The apparatus of claim 8, wherein:

the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13)

10. The apparatus of claim 1, particularly for use with a computing system that has plural processors (column 9, line 6 through column 10, line 21).

11. The apparatus of the claim 1, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 6-17):

at least three data collecting and responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 55-60).

12. Apparatus of the claim 1, particularly for use with such system that is substantially exclusively made up of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (column 12, lines 20-55).

13. Apparatus for deterring failure of a computing system, wherein the computing subsystem optionally includes plural mutually redundant modules (column 9, lines 41-56); said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60), wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules if present (Figures 1 and 3 show a distinct separation between the MP and IO modules);

the circuits comprising portions for identifying failure of any of the circuits and correcting for the identified failure (column 2, lines 55-60).

14. The apparatus of claim 13, wherein: the program-operating portions comprise a section that corrects for the identified failure by taking a failed circuit out of operation (column 2, lines 5-14).

15. The apparatus of claim 14, wherein: the program-operating portions comprise a section that substitutes and powers up a spare circuit for a circuit taken out of operation (column 3, lines 51-56).

17. The apparatus of claim 13, wherein:

the program-operating portions comprise at least three of the circuits (column 2, line 1); and

failure is identified at least in part by majority vote among the at least three circuits (column 2, lines 55-60).

18. The apparatus of claim 13, particularly for use with a computing system that has at least one software subsystem for conferring resistance to failure of the system(column 7, lines 63 through column 8, lines 6); and wherein:

the circuits comprise substantially no portion that interferes with such failure-resistance software subsystem (no such interference is disclosed, and such interference would be contrary to the intent of the disclosure).

20. The apparatus of claim 13, particularly for use with a computing system that has plural generally parallel computing channels (column 2, lines 1-4); and wherein:

the circuits comprise portions for comparing computational results from such parallel channels (column 2, lines 5-8).

21. The apparatus of claim 20, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

22. The apparatus of claim 13, particularly for use with a computing system that has plural processors (column 2, lines 17-22); and wherein:

the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 55-61).

23. The apparatus of claim 13, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 55-60).

25. Apparatus for deterring failure of a computing system that has at least one software subsystem for conferring resistance to failure of the system; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60);

the circuits comprising substantially no portion that interferes with such failure-resistance software subsystem (no such interference is disclosed, and such interference would be contrary to the intent of the disclosure).

26. The apparatus of claim 25, further comprising: such computing system, including such at least one software subsystem (column 2, lines 4-5).

28. The apparatus of claim 25, particularly for use with a computing system that has plural generally parallel computing channels; and wherein (column 2, lines 1-4): the circuits comprise portions for comparing computational results from such parallel channels (column 2, lines 5-8).

29. The apparatus of claim 28, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

30. The apparatus of claim 25, particularly for use with a computing system that has plural processors (column 9, line 6 through column 10, line 31); and wherein:

the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 55-61).

31. The apparatus of claim 25, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17)), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 55-60).

42. Apparatus for deterring failure of a computing system that is distinct from the apparatus and that has plural generally parallel computing channels; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 55-60); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60) wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules if present (Figures 1 and 3 show a distinct separation between the MP and IO modules);;

the circuits comprising portions for comparing computational results from such parallel channels (column 2, lines 55-60).

43. The apparatus of claim 42, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

44. The apparatus of claim 42, wherein: the comparing portions comprise at least one section for analyzing discrepancies between the results from such parallel channels (column 2, lines 55-60).

45. The apparatus of claim 44, wherein: the comparing portions further comprise at least one section for imposing corrective action on such system in view of the analyzed discrepancies(column 2, lines 55-60).

46. The apparatus of claim 45, wherein: the at least one discrepancy-analyzing section uses a majority voting criterion for resolving discrepancies (column 2, lines 55-60).

48. The apparatus of claim 47, wherein: the parallel channels of the computing system are of diverse design or origin (column 2, lines 1-13 as the channels originate from different sources, they are independent of origin).

49. The apparatus of claim 48, wherein

the comparing portions comprises circuitry for performing an algorithm to validate a match that is inexact (column 2, lines 5-8: the analog case)

52. The apparatus of claim 42, particularly for use with a computing system that has plural processors (column 2, lines 4-6; and wherein:

the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 23-37).

53. The apparatus of claim 42, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 5-60).

55. Apparatus for deterring failure of a computing system that has plural processors; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22), wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules if present (Figures 1 and 3 show a distinct separation between the MP and IO modules; column 9, lines 15-30); and

circuits of the network for operating programs to guard such system from failure(column 2, lines 55-60);

the circuits comprising portions for identifying failure of any of such processors and correcting for identified failure (column 2, lines 55-60).

56. The apparatus of claim 55, wherein: the identifying portions comprise a section that corrects for the identified failure by taking a failed processor out of operation (column 2, lines 5-14

57. The apparatus of claim 56, wherein: the section comprises parts for taking a processor out of operation only in case of signals indicating that the processor has failed permanently (all failures in the system of Rasmussen are permanent such is the degree of fault tolerance demanded).

58. The apparatus of claim 55, wherein: the identifying portions comprise a section that substitutes and powers up a spare circuit for a processor taken out of operation (column 2, lines 24-27).

60. The apparatus of claim 55, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (column 2, lines 16-17):

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 16-17).

62. Apparatus for deterring failure of a computing system; said apparatus comprising:

a network of components having terminals for connection to such system (column 2, lines 14-22); and

circuits of the network for operating programs to guard such system from failure (column 2, lines 55-60);

the circuits comprising modules for collecting and responding to data received from at least one of the terminals (column 2, lines 55-60), said modules comprising:

at least three data-collecting and -responding modules (column 2, lines 16-17), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 2, lines 16-17);

wherein the network, including all of the modules and all of the processing sections, is constructed to be initially and permanently distinct from such computing system including all of such redundant modules if present (Figures 1 and 3 show a distinct separation between the MP and IO modules; column 9, lines 41-54);

Allowable Matter

Claims 50 and 51 remain objected to while containing allowable subject matter as set forth in the previous Official Action.

Applicant is reminded the claims are indicated as allowable as a whole including any intervening base claims.

Response to Applicant Arguments

I. The IDS is now considered. The Initialed PTO-1449 is attached.

II. The Examiner maintains the objection of claim 48 as a duplicate claim of claim 43. "Such computer" is recited twice in the body of the claim and is protected by the claim. See the rejections and responses concerning 35 USC §112, fourth paragraph for further explanation.

III. A. The first set of rejections under 35 USC §112, second paragraph have been withdraw.

B. The rejections of the second set of claims (claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64 and 65) remain. The Examiner is still unable to determine the bounds of the claims. While a product produced for sale/profit and removed from a shelf is clearly covered, where the coverage stops is at issue. Cited as an example in the rejection above is practice of over clocking. Additional examples which the Examiner is unable to determine coverage for are: products which are commercially custom ordered en-mass, products not produced commercially but still sold, and products not distributed in an off-the-shelf manner.

C. Despite lengthy argument and legal analysis (and in fact partially due to it), the Examiner remains genuinely uncertain of the scope of the claimed subject matter.

IV. The Examiner maintains the 35 USC §112, fourth paragraph rejections. Applicant has claimed a computer system in the body of the claims twice and even elaborated on the computer in the body of the claims. AS such Applicant has coverage for the computer in that environment. Further, each claim's preamble sets forth the specific invention as "An apparatus". Should Applicant wish specific coverage for the computer system, Applicant should file independent claims with a preamble which recites such the computer system as the invention.

V. Beginning on page 28, Applicant makes some general allegations not directed to any specific claim. The Examiner believes these arguments pertain most directly to claim 1.

A. Applicant argues there are not terminals in the cited reference. The Examiner points out that given the presence of connections, the communication paths must connect to the MP and IO modules. The point of these connections is a terminal, barring any exotic, undisclosed, unclaimed functionality from Applicant.

B. Applicant alleges that the parallel redundancy of the reference does qualify as pertinent art. The Examiner points out that both the MP modules and IO modules and the components within the IO modules are all redundant and thus do in fact read on the claimed invention.

C. Applicant argues that C-nodes as defined in the specification are not present. The Examiner points out that C-nodes as defined in the specification are not specifically claimed. The reasonable breath of the claims includes the defined C-nodes but is not limited to them.

D. Applicant argues that the M-nodes of the specification are not present. The Examiner once again points out that M-nodes are not claimed, simply a "network of components."

VI. Applicant argues that rejection of claim 13 does not properly take into account the distinction between the network of components and the computer system they protect. The Examiner points out Figure 1, where the MP modules (item 1) are distinct from the I/O modules (2). This is a simple block view which distills the information in the remaining 25 more complicated figures. Applicant is invited to view the remaining figures, however Applicant with discover the MPs of the Main Processor are consistently distinct from the I/O modules.

VII. As per claim 42, Applicant argues that MP being parallel contracts the claimed invention. Applicant is reminded that MPs, while in parallel, meet the limitations of the network of components, the I/O modules meet the breadth of computer system which are also in parallel, and in fact the communication channels from the I/O modules are redundant and in parallel.

VIII. As per claim 55, Applicant argues that the reference lacks the proper plural processors in the correct position. The Examiner points out that the I/O modules (the computer system) has plural processors that operate in parallel (column 9, lines 15-30). Applicant seems to consider the MP modules the computer system and network of components for the claimed invention when in fact the MP modules are the "network" and the I/O modules are the "computer system".

IX. As per claim 62, Applicant once again argues the distinct nature of the "network" and "computer." The Examiner points to Figure 1, where the MP modules (item 1) are distinct from the I/O modules (2). This is a simple block view which distills the information in the remaining 25 more complicated figures. Applicant, once again, invited to view the remaining figures, however Applicant with discover the MPs of the Main Processor are consistently distinct from the I/O modules.

X. Applicant makes multiple arguments regarding the insufficiency of rejection of claim 25. They are addressed separately below.

A. Page 9 contains a full rejection of claim 25 under 35 USC §102(e). The claim appears to have simply been lost in the headers through out the rejection. As the rejection was present, properly written and in the correct location, this minor error is insufficient to prevent this action from being made final.

B. Applicant argues that the reference does not explicitly recite avoid all interference. Applicant recites a passage describing anti-tampering (interference) specifically for fault tolerance. As Applicant is well aware, the claim contains the additional limitation "substantially." As no bounds are provided for how much "substantially no portion" actually is, the Examiner has determined that the disclosed passage clearly provides for "substantially no portion that interferes." Applicant's arguments in the previous two responses and lengthy recitation of case law support this finding.

XI. Applicant cites a high cost to pursuing this application. Since the initial filing, the only fees levied by the USPTO have been two requests by Applicant for Extensions of Time, at the small entity rate, of $55 on 8/16/04 and $225 on 4/25/05. If Applicant has paid fees to the government in excess of those listed, a refund may be in order. Regarding high cost to the government, it is to the publics benefit for a full and complete examination prior to allowance of any patent, as the cost of invalid patent incalculable.

Final Disposition

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Primary Examiner
Art Unit 2114